IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION

REDSTONE LOGICS LLC, Plaintiff, v. QUALCOMM INC. and QUALCOMM TECHNOLOGIES, INC. Defendants.	Case No. 7:24-cv-000231-ADA

PLAINTIFF'S SURREPLY CLAIM CONSTRUCTION BRIEF

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I. TERM 1: "THE FIRST CLOCK SIGNAL IS INDEPENDENT FROM THE SECOND CLOCK SIGNAL"

'339 Patent Claims	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 1, 21	**Plain and ordinary meaning**	**Plain and ordinary, meaning, where the plain and ordinary meaning requires that the first and second clock signals depend from different reference oscillator clocks**

Qualcomm's construction has no support beyond the arguments it wishes the applicant had made in prosecution. Indeed its "simpler" construction has even less support than the construction this Court previously rejected. While Redstone inadvertently identified NXP's "provided by" construction, as Qualcomm makes the same faulty arguments as NXP did, nothing changes. Qualcomm's construction still focuses on a third clock signal never contemplated in the claims, ignores how the applicant used the amendments to overcome Jacobowitz, and rewrites the applicant's discussion of Kim. Qualcomm's "demonstrative example" is even worse, having no intrinsic or reliable extrinsic support and is counter to Qualcomm's own evidence. Because the independent term is concerned with the relationship between the first clock signal and the second clock signal, not any other signals or components, Qualcomm's construction should be rejected.

First, Qualcomm bears the burden to show a "clear and unmistakable disclaimer." *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1063–64 (Fed. Cir. 2016). But Qualcomm's creative interpretation of the file history around Kim hardly amounts to anything "unequivocal[]" as it claims. The applicant identified two limitations Kim failed to disclose and explains instead of meeting *both* sets of limitations, *Kim* disclosed an apparatus providing clock signals to each of the cores:

File History – Response to Office Action 8/29/2012

In addition, *Kim* also fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal, respectively. In addition, the first clock signal is independent from the second clock signal. Instead, *Kim* discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having a single clock source (i.e., 170 in FIG. 1 or 270 in FIG. 2). The clock signal from this single clock source is then processed (i.e., divided or multiplied) and provided to each of the cores. See *Kim*, paragraphs [0024]-[0025] and FIGs 1 – 2.

Dkt. 29 at 2 (citing Ex. H at 10-11). Qualcomm's attempt to create a separate argument that only considers the underlined text, is an improper circumvention of the requirement for a "clear and unmistakable disclaimer." *See Omega Eng'g, Inc, v. Raytek Corp.*, 334 F.3d 1314, 1326 (Fed. Cir. 2003). Instead, the applicant's statements "must always receive consideration in context." *Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1378 (Fed. Cir. 2008). Here the context is clear that "independence" is not tied to the origin of the signals.

When introducing the "independent" limitation, the Applicant had faced with rejection in light of Jacobowitz's single V_R clock signal as input to local oscillators. Dkt. 27-7. This is clearly the context and target of the amendment as it was what the applicant expressly discussed with the examiner in an interview. *See* Dkt. 27-8. If, as Qualcomm contends, the focus of "independent" was on the origin of the clock signals, the applicant would have argued that distinction as to both Jacobowitz and Kim. But Qualcomm does not, because it cannot, base its argument on Jacobowitz. *See* Dkt. 29 at 2-3 ("the *Jacobowitz* reference[] is not even the basis of Qualcomm's claim construction position"). Despite also having a single clock source, *see* Dkt. 27-5 at Fig. 6, the Applicant never made even a colorable argument that Jacobowitz failed to disclose "independent" clock signals because of the singular source. This context is damning to Qualcomm's argument.

The other key context to "independent" is how the Applicant uses the term elsewhere. The applicant uses it, whether describing voltage or clock signals, to explain only that without sets of processor cores, the claimed signals do not exist. *See* Dkt. 27-9 at 11 ("neither Jacobowitz nor Kim discloses having sets of processor cores configured to receive multiple and independent clock signals"). This is the only consistent use of "independent": where there are no sets of processor cores, there are not claimed independent clock signals or voltages. *See id*. at 10 ("Kim fails to disclose…a first supply voltage and a second supply voltage, which is independent from the first supply voltage, respectively. Instead, Kim discloses having each core, not a set of processor cores, received a V_{DD} (i.e., V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4})"), *id*. at 10-11 ("Kim also fails to disclose … the first clock signal is independent form the second clock signal. Instead, Kim discloses … [t]he clock signal from this single clock source is … provided to each of the cores"); *see also id*. at 9 ("Jacobowitz merely mentions that '[f]urther power management can be realized by controlling the power supply voltage (Vdd) to each core and/or chip.' In other words, Jacobowitz is silent with respect to least [sic] the recited different sets of processor cores configured to receive independent supply voltages")(emphasis in original). Without a single disclaimer as narrow as Qualcomm's proposed construction, that construction should be rejected.

Qualcomm's remaining argument also fails for want of support. In essence, Qualcomm argues because 1) a POSITA would only consider a system with a single oscillator producing a variable frequency; and 2) any two frequency functions that include a common variable cannot be independent, clock signals based on a single oscillator cannot be independent. *See* Dkt. 27 at 5-8. There is no support for either.

On the first, Qualcomm can only cite Kim, but Kim teaches ensuring a particular frequency, an incompatible goal with a variable input frequency that is not otherwise stabilized. Although

Qualcomm originally cited only Dr. Villasenor, Dkt. 27 at 5-8, those opinions are entirely conclusory, Dkt. 28 at 6-7, so Qualcomm now relies solely on Kim, *see* Dkt. 29 at 4-5. But Kim does not support Qualcomm either. First, Kim explains signals 262, 264, 266, and 268 are "***an*** input clock frequency from the main PLL 260" "which provides ***a first*** multiple of the clock frequency provided by the clock source." Kim at [0025] (emphasis added). While Kim does describe that the further PLLs deliver "a reference input clock frequency … that is further multiple of the clock frequency provided … by the clock source," Kim explains "a respective PLL is configured to provide a reference input clock frequency[] to a respective core K to ensure that a respective operational or operating core frequency of the respective core is at least equal to the adjusted reference input clock frequency." *Id*. Kim's respective PLLs are configured to ensure a particular frequency to each core. *Id*.; *see also id*. ("a specification core frequency[] is preset or pre-specified for each of the cores…"). Qualcomm's simplistic example is incompatible with ensuring a specific frequency, as is the central point of Qualcomm's argument. A change in the oscillator frequency would cause a change in the frequency delivered to the component. *See* Dkt. 27 at 6. A real system would stabilize the oscillator frequency, either ensuring it is not variable or that its variance is addressed by a later component.

On the second point, Qualcomm followed the same failing trend initially relying only conclusory testimony from Dr. Villasenor before contending Kim provides support. But neither do. As explained in Redstone's response brief, Qualcomm has not shown a POSITA has ever considered "independence" of two signals relies on an upstream signal. And the only non-conclusory testimony provided by Dr. Villasenor would render any two signals on a single device not independent. *See* Dkt. 28 at 8. As to Kim, Qualcomm's reliance is circular. Kim does not on its own provide anything to support the notion that a common variable in two signals render those

signals not independent. Only if the Court were to find the Applicant or the Examiner found any signals were not independent, rather than that there were no claimed signals associated with sets of cores, could Kim support this point. But as explained above, neither the Applicant nor the Examiner ever took that position. Without support for either of these two necessary contentions, Qualcomm's "demonstrative example" is meritless.

Qualcomm's claim construction has no support and focuses on irrelevant upstream components, this term should be given its plain meaning. The Court should adopt its prior construction of this term: "plain-and-ordinary meaning, wherein the plain meaning does not require that the first and second clock signals depend from different reference oscillator clocks." Dkt. 27-11 at 2.

II. TERM 2: "LOCATED IN A PERIPHERY OF THE MULTI-CORE PROCESSOR"

Here, Qualcomm fails to meet its burden of proof. First, as Qualcomm effectively concedes, the intrinsic record demonstrates no ambiguity or indefiniteness. This should be the end of the inquiry. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) ("[W]here the public record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper."). But even if the Court considers Qualcomm's extrinsic evidence, it is insufficient, procedurally defective, and/or indeed actually supports Redstone's position. Because of these evidentiary defects in Qualcomm's construction, the Court should give "located in a periphery of the multi-core processor" it's plain and ordinary meaning.

Qualcomm does not and cannot allege there is any confusion as to the scope of "periphery" or "multi-core processor" based on the intrinsic record. In its opening brief, Qualcomm acknowledges the example multi-core processor in Figure 1 but immediately jumps to a counter example provided by its expert. Dkt. 27 at 14. But such is improper. The Federal Circuit has long

held that extrinsic evidence is secondary to the intrinsic record. *See e.g. Vitronics*, 90 F.3d at 1583; *Intel Corp. v. VIA Techs., Inc.*, 319 F.3d 1357, 1367 (Fed. Cir. 2003) (when a claim "is not indefinite as construed from intrinsic evidence, [] reference to extrinsic evidence is improper."). While Qualcomm alleges the intrinsic record is "simplified and idealized," Dkt. 29 at 6, that does not show any ambiguity in the intrinsic record. Instead, Qualcomm can only provide "Qualcomm and Dr. Villasenor have already explained why that is not the case." *Id*. But such demands the Court to look to the extrinsic first and is thus improper.

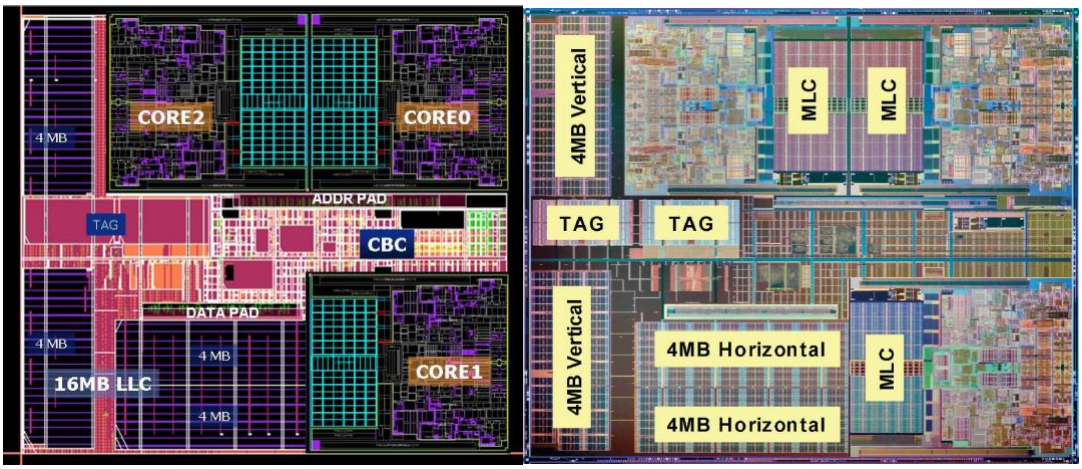
Even if the Court were to consider the extrinsic evidence, it still fails to meet Qualcomm's burden. "Any fact critical to a holding on indefiniteness, moreover, must be proven by the challenger by clear and convincing evidence." *Intel Corp. v. VIA Techs., Inc.*, 319 F.3d 1357, 1366 (Fed. Cir. 2003). But Qualcomm can only provide self-serving, conclusory expert testimony. Instead of showing what a POSITA might be faced with and explaining the confusion it would cause, Dr. Villasenor shuffles blocks around with no regard for what a functioning processor might require. *See* Dkt. 27 at 14-15 (providing supposed multi-core processors without the requisite voltage or clock infrastructure or caches). Dr. Villasenor's entire support for these figures being realistic is to simply conclude the arrangement would be "not [] unusual" given "real estate" constraints. Dkt. 27-1 at ¶71. Qualcomm's argument[1] that the voltage and clock infrastructure are the blocks Dr. Villasenor is attempting to locate, Dkt. 29 at 6-7, misses the point. Because it is the only basis for "periphery" being ambiguous is this example, Qualcomm must show that a POSITA would actually consider a processor with cores haphazardly strewn around a die to support its

[1] Qualcomm's other counter argument that Redstone only offers attorney argument based on the statements of what a POSITA would understand are inapposite. Each of those statements are supported either by citation to the intrinsic record or simple logic like a POSITA would only consider a functional processor when considering the claims. Redstone's choice not to use an expert to parrot its arguments as Qualcomm did, does not render these arguments improper.

conclusion that a periphery would be impossible to ascertain in such an example. Asking questions about where a control block, not to mention the often complex and no less important wiring arrangement, would be placed does not show a what a POSITA would consider.

Seemingly recognizing its deficiency, Qualcomm raises additional extrinsic evidence. *See* Dkt. 29 at 8. But this exhibit was never disclosed as part of exchange of extrinsic evidence. Ex. A at 5. Qualcomm identified two dictionaries, three expert declarations, and Redstone's Patent Owner's Preliminary Response in MediaTek's IPR but no Intel Technology Journal. *Id*. Because Qualcomm failed to properly disclose this evidence and raised it for the first time in its reply, Redstone requests both Ex. 6 and Qualcomm's related arguments be struck.

To the extent the Court declines to strike Ex. 6, it only supports Redstone's position that multi-core processors are not so simple as Dr. Villasenor's figures. Unlike his arbitrary arrangement of sets of cores on a die with an interface block and wiring placed with no disclosed logic, Intel's arrangement is highly ordered:



Dkt. 29-2 at 232-33. This arrangement is hardly similar to what Dr. Villasenor proposed. While Intel recognized a "unique physical design challenge[]," the result was a compact and logical arrangement, not sets of cores placed well away from each other with no supporting infrastructure.

Intel arranged its sets of cores[2] tightly with the associated Mid-Level Caches. *See id.*; *see also id.* at 230 ("The Dunnington processor has three levels of caches: … 3MB of non-inclusive Mid-Level Cache (MLC) for each CMP core-pair…"). Likewise the Last Level Cache (LLC) and the Caching Bridge Controller (CBC) that integrate the CMP core-pairs, are arranged directly adjacent to the core-pairs. *Id.* at 230. This culminates in a compact, rectangular multi-core processor whose periphery is obvious and highlights why Dr. Villasenor's opinions are unpersuasive.

Because Qualcomm has not and cannot meet its burden of proof, the Court should give this term ITS PLAIN AND ORDINARY MEANING.

III. TERM 3: "LOCATED IN A COMMON REGION THAT IS SUBSTANTIALLY CENTRAL TO THE FIRST SET OF PROCESSOR CORES AND SECOND SET OF PROCESSOR CORES"

Last, the intrinsic record provides the metes and bounds of this term. As Qualcomm concedes, "common region" is simply the area shared by the claimed sets of cores. This "common region" being "substantially central" to those claimed sets of cores is likewise clear from reference to the specification and its grammar. Together they provide a construction "wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region of the first set of processor cores and the second set of processor cores." While broad, this construction is not indefinite.

It is plain from the patent that a "region" is merely a subdivision the multi-core processor containing a set of cores. *See* '339 Patent at 2:20-27. Modified by "common" in a claim including two sets of cores, its meaning is clear, the subdivision of the multi-core processor containing both sets of cores. While Qualcomm disputes these points, it concedes "a POSITA understands this

[2] Redstone does not suggest any of the Intel architecture meets any limitation of the claims, but rather adopts, arguendo what Qualcomm appears to suggest would be considered by a POSITA.

phrase means the first and second sets of processor cores share a common region where control blocks are located." Dkt. 27 at 19-20.

Qualcomm's concession that it understands "common region" is the proverbial nail in the coffin. Whether it is called "claim differentiation" or "[t]he general presumption that different terms have different meanings," it is a presumption and "where neither the plain meaning nor the patent itself commands a difference in scope between two terms, they may be construed identically," not indefinitely. *See Power Mosfet Technologies, L.L.C. v. Siemens AG*, 378 F.3d 1396, 1409–10, 72 U.S.P.Q.2d 1129 (Fed. Cir. 2004). Common region is not indefinite and Qualcomm has not met its burden to show otherwise.

Qualcomm's efforts to find indefiniteness from the rest of the term is no more effective. First, there is no "grammatic ambiguity," there is only Qualcomm's mistake in the first instance. The claim reads "… control blocks located in a common region that is substantially central…" '339 at Cl 14. If "substantially central" applied to "control blocks" it would be an "are" not an "is" as control blocks is plural while common region is singular. This is on top of the simple ordering of phrases. Second, "substantially central" is sufficiently explained in the patent. The specification provides for the placement of control blocks, also the subject of claim 14, "in a common area located near the center of the multi-core processor." '339 Patent at 2:31-40. This language mirrors the claim and clarifies by contrast an area located near the center from the sides of the processor. *See id*. Likewise, in the claim itself, because a "region" is a subdivision of the processor containing a set of cores and the "common region" is the region containing both sets, that a "common region" to be "substantially central" to those sets the term becomes a tautology. A group of two things is always substantially central to those things. In effect the claim only requires there to be a common region of the sets of cores and that the control block be placed in it. While the "substantially central" limitation may be superfluous, that is the plain meaning of the term. And when there is no basis for altering the plain

meaning, superfluity cannot alter that meaning. *See Power Mosfet*, 378 F.3d at 1409–10. As such, Qualcomm's indefiniteness position is inappropriate.

To the extent the Court feels this term must be construed, it should be construed as: The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region of the first set of processor cores and the second set of processor cores.

IV. CONCLUSION

For the reasons provided above, all disputed terms should be given their plain and ordinary meaning. Defendant has failed to meet its burden to show any term is indefinite.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I certify that on May 23, 2025, a true and correct copy of the foregoing document was electronically filed with the Court and served on all parties of record via the Court's CM/ECF system.

/s/ Reza Mirzaie
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